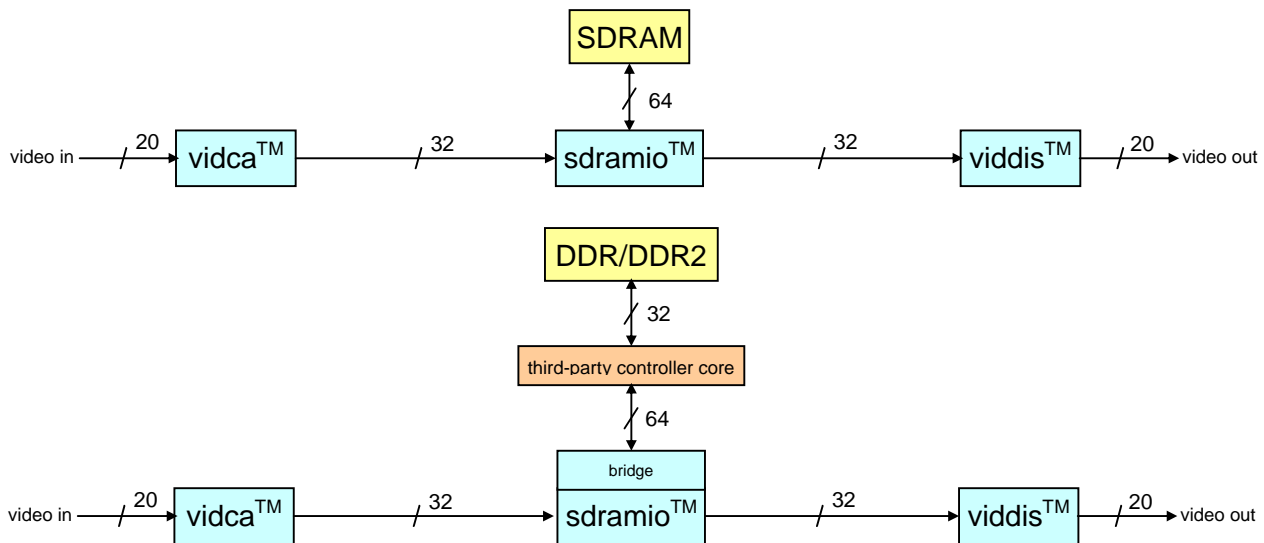


High-Definition Frame Delay

This video solution shows how to use Core Values™ cores to create a High-Definition Frame Delay.

FEATURES

- Delays as many frames as desired.
- Interfaces to 1080i or 720p 4:2:2 YCbCr 20-bit data
- Uses vidca™ and viddis™ video capture and display
- sdramio™ connects directly to SDRAM memory or via bridge to third-party DDR/DDR2 controller cores
- Linted and Verified Verilog 2001 Source Code
- Permanent Company License (not per-project)
- ASICs and Actel, Altera, Lattice and Xilinx FPGAs

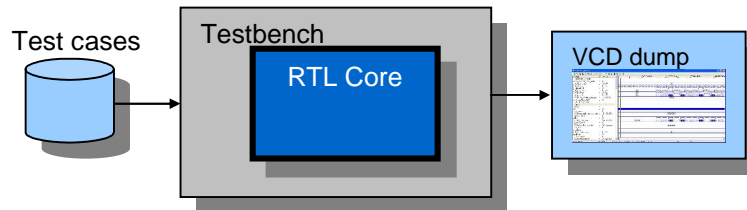


EXTERNAL REQUIREMENTS

- Active-low Resets, 74.25/1.001 MHz HD clock, SDRAM/DDR/DDR2 clock
- Third-party controller core for DDR/DDR2

DELIVERABLES FOR EACH CORE

- Synthesizable Verilog 2001 RTL Source Code
- VCD Functional Dump
- Fast Verilog 2001 Testbench and Test cases
- User Manual



APPLICATIONS

- MPEG/VC-1/H.264 Encoding
- Audio-Video Synchronization
- Special Effects