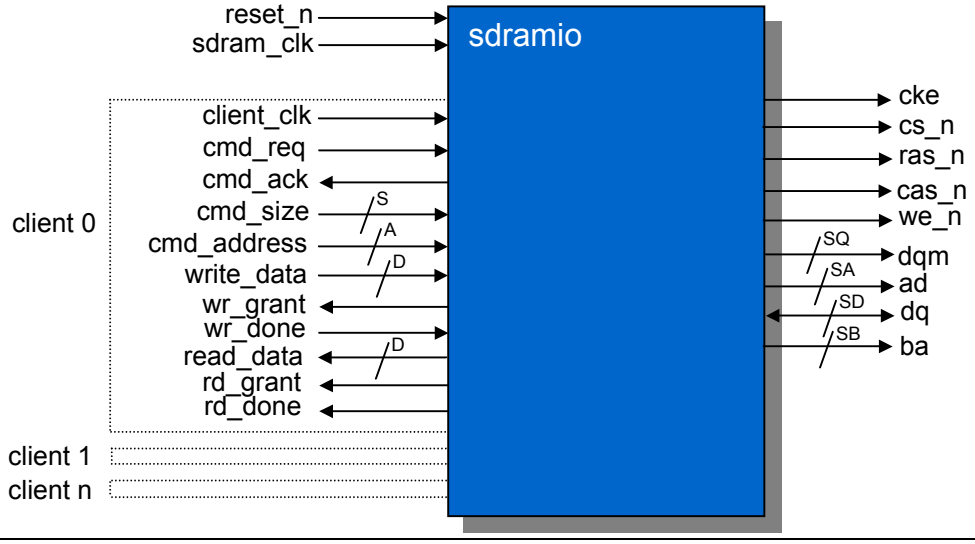
video-cores

High-performance SDRAM Controller core: sdramio™

This silicon proven Core Values™ encoder allows designs with multiple memory clients to interface directly to SDRAM memories. Its Arbiter can easily be ported to a DDR/DDR2/DDR3 design.

FEATURES

- Interfaces directly to SDRAM memory ICs of multiple widths and depths
- Hides SDRAM latency by having separate command, write and read queues
- 200+ MHz performance
- Simple and fast synchronous multi-clock, multi-client interface
- Separate clocking for client interface prevents high-speed requirements all over the integrated circuit
- Separate control, client and sdram clock domains and resets. Different clocks per client.
- Parametrizable for address and data sizes and number of clients
- Linted and Verified Verilog 2001 Source Code
- Permanent Company License (not per-project)
- Targeting ASICs and Actel, Altera, Lattice and Xilinx FPGAs

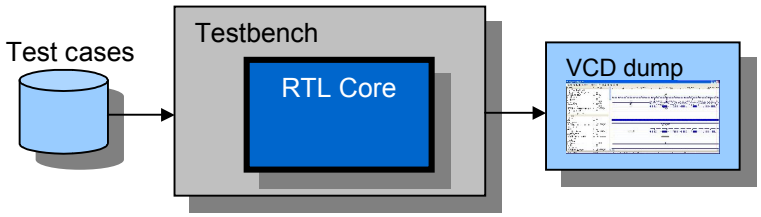


EXTERNAL REQUIREMENTS

- Client, control and SDRAM clocks and resets

DELIVERABLES

- Synthesizable Verilog 2001 RTL Source Code
- Fast Verilog 2001 Testbench and Test cases
- VCD Functional Dump
- User Manual



APPLICATIONS

- High-performance SD/HD video chips
- High-performance Networking chips
- High-performance Audio chips
- Cell Phone chips

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