

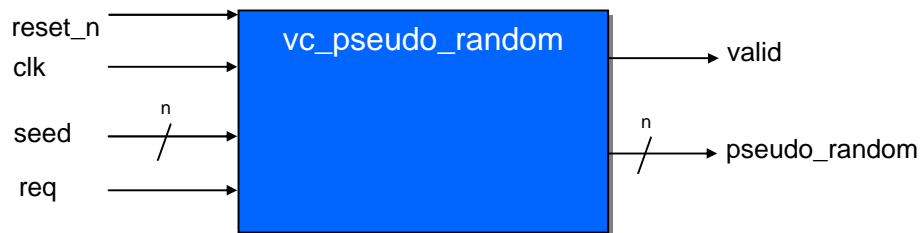


Pseudo-Random Number Generator: vc_pseudo_random

This Core Values™ pseudo-random number generator of width n bits (n = 3 .. 32), has the unique capability of producing all 2ⁿ values per any 2ⁿ request cycles.

FEATURES

- Output bit width n is parameterized between 3 and 32 bits
- Asynchronous low reset signal (reset_n), followed by synchronous release
- Generated values are deterministic per an initial seed value, which has the same bit width as the output.
- For every 2ⁿ requests, 2ⁿ unique values are generated (a sequence).
- The 2ⁿ+1th generated value is NOT identical to either the first nor the last value in the previous sequence.
- A series of 2ⁿ-1 unique sequences of 2ⁿ unique values can be generated, before the entire output repeats itself.
- Linted Verilog 2001 Source Code Available
- Per-project Netlist or Permanent Licenses
- Targeting ASICs and Actel, Altera, Lattice and Xilinx FPGAs

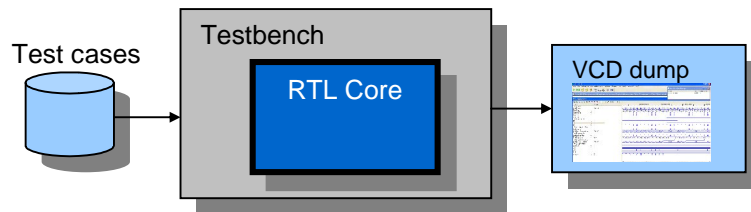


EXTERNAL REQUIREMENTS

- Clock, Active-low reset

DELIVERABLES

- Synthesizable Netlist or Verilog 2001 RTL
- Verilog 2001 Testbench and Test cases
- C Model Source Code and a Windows Executable
- VCD Functional Dump
- User Manual



APPLICATIONS

- Professional Audio/Video Transmission
- Professional Video Processing
- Prosumer Standard-definition Devices
- Rack-mounted Media Systems