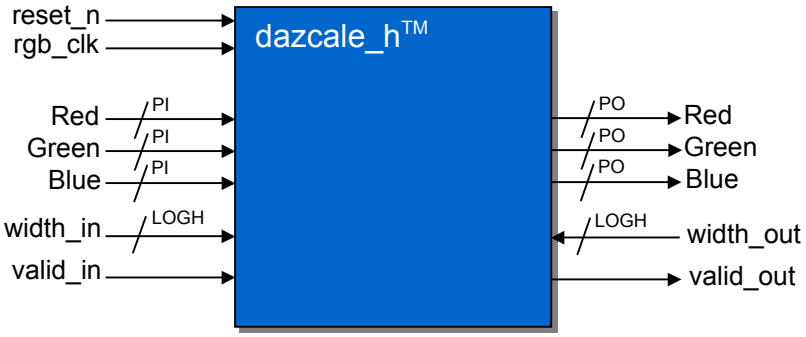
video-cores

High-Performance Parametrizable RGB Horizontal Down Scaler: dazcale_h™

This Core Values™ product horizontally down-scales interlaced or progressive images. The core is customized for your specific application and no logic is wasted on resolutions that are not needed. For example you can start with an SD NTSC input (720x487i) and horizontally down-scale to a VGA sized output (640x487i) for more efficient MPEG/H.264 encoding or to adapt to a certain display Horizontal resolution. Implementations are available with single-macroblock resolution and precision is parametrizable for quality/size decisions.

FEATURES

- Down-scales directly RGB images of any bit depth
- Interfaces to 4:4:4/4:2:2 YCbCr data with converters
- Customized to any desired input/output size
- Converts between square and rectangular pixels
- Parametrizable Input, Processing, Output precision
- Macroblock boundaries: 720:704, 720:640, etc
- Sample output images available for evaluation
- Linted and Verified Verilog 2001 Source Code
- Permanent Company License (not per-project)
- ASICs and Actel, Altera, Lattice and Xilinx FPGAs

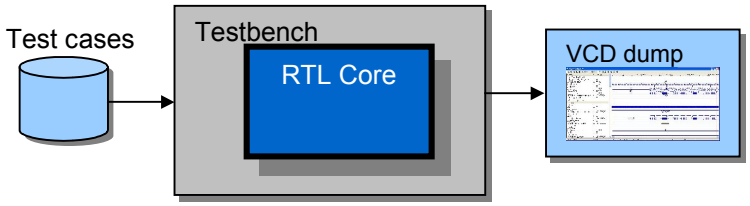


EXTERNAL REQUIREMENTS

- Reset, Input Clock and Output Clock
- Memory (core is customized to interface)

DELIVERABLES

- Synthesizable Verilog 2001 RTL Source Code
- Fast Verilog 2001 Testbench and Test cases
- VCD Functional Dump
- User Manual



APPLICATIONS

- MPEG/H.264 Encoding
- Consumer Electronics Video/Graphics
- Professional Video/Graphics
- Cell phone Video/Graphics

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