

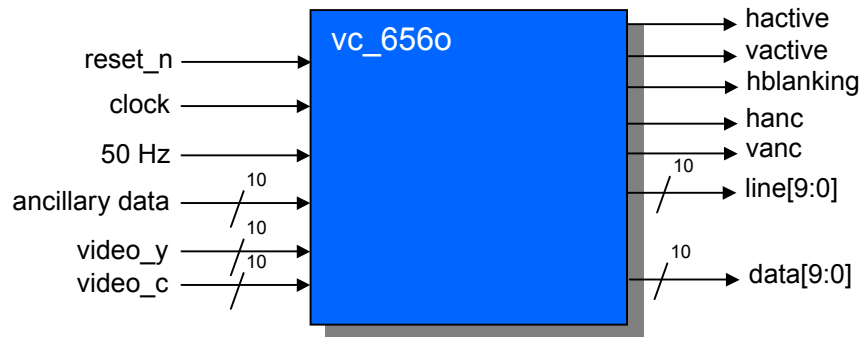


ITU-R 656-4 Encoder: vc_656o

This Core Values™ encoder allows designs with internal 4:2:2 YCbCr Standard Definition 20-bit video and 10-bit ancillary data buses connect to devices that receive ITU-R 656 27MHz NTSC and PAL 10-bit data with embedded syncs.

FEATURES

- Encodes to ITU-R 656-4
- Supports 50Hz/625 and 60/525 video
- Acts as master to video-and-data-plus-sync logic
- Signals HANC and VANC ancillary data periods for data insertion
- Clamps active video to valid non-sync values
- Linted Verilog 2001 Source Code
- Permanent Company License (not per-project)
- Targeting ASICs and Actel, Altera, Lattice and Xilinx FPGAs

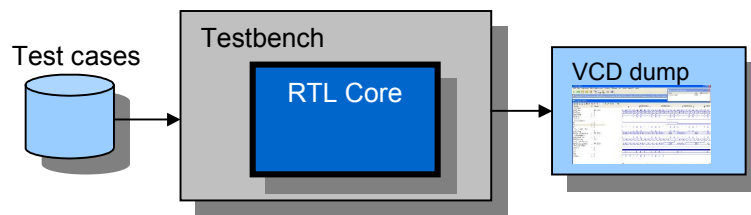


EXTERNAL REQUIREMENTS

- 27 MHz clock and active-low reset
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DELIVERABLES

- Synthesizable Verilog 2001 RTL Source Code
- Verilog 2001 Testbench and Test cases
- VCD Functional Dump
- User Manual



APPLICATIONS

- Professional Audio/Video Transmission
- Professional Video Processing
- Prosumer Standard-definition Devices
- Rack-mounted Media Systems